is a range from 450 to 750°C.

71. (New) A method according to claims 24 wherein said semiconductor device comprises a CPU.

72. (New) A method according to claims 32 wherein said semiconductor device comprises a CPU.

73. (New) A method according to claims 41 wherein said thin film transistor is used in a CPU.

74. (New) A method according to claims 50 wherein said semiconductor device comprises a CPU.

75. (New) A method according to claims 56 wherein said semiconductor device comprises a CPU.

REMARKS

Applicants wish to thank the Examiner for the very thorough consideration given the present application. The Office Action of ***December 6, 2000*** and Notice of Non-Compliant Amendment of May 13, 2001 has been received and its contents carefully noted. Filed concurrently herewith is a *Request for a Three (3) Month Extension of Time* that extends the shortened statutory period for response to ***June 6, 2001***. Accordingly, Applicants respectfully submit that this response is timely filed.

Claims 24-63 were pending in the present application prior to the aforementioned amendment. By the above actions, claims 24, 32, 38, 41, 47, 50, 56 and 59-63 have been amended and new claims 64-75 have been added to better encompass the full scope and breadth of the invention notwithstanding, Applicants belief that the claims would have been allowable as originally filed. Accordingly, Applicants assert that no new matter has been added and no claims have been narrowed within the meaning of *Festo*. Accordingly, claims 24-75 are pending herein, and, for the reasons set forth in detail below, are believed to be in condition for allowance.

Initially, the *Office Action* appears to reject claims 31, 38, 40, 47, 49, 55 and 59-63 under U.S.C. §112, second paragraph as being indefinite. Due to the above actions, claims 38, 47 and 59-63 have been amended to overcome the rejection. More particularly, claims 38 and 47 have been amended to recite --wherein said irradiating step is performed in a nitrogen atmosphere--, and claims 59-63 have been amended to recite --said temperature--. Applicants respectfully traverse the apparent rejection of claims 31, 40, 49 and 55. As described in the specification on page 18, lines 4-7, when the laser light is irradiating the semiconductor film, the surface of the semiconductor film is in a melted state and then crystal growth <u>in minute portions</u> of the semiconductor film is accelerated. Accordingly, crystallinity of the semiconductor film as a whole can be improved by the irradiation step. Reconsideration and withdrawal of the rejection is requested in view of the aforementioned amendments and remarks.

The *Office Action* rejects claims 56-58 under 35 U.S.C. §112, first paragraph as being nonenabling. Due to the above actions, claim 56 has been amended so as to recite --crystallizing said semiconductor film by first heating using a catalyst material--. Reconsideration and withdrawal of the rejection is requested in view of the aforementioned amendments and remarks.

The *Office Action* rejects claims 24-63 under 35 U.S.C. §112, first paragraph as containing new matter. Applicants respectfully traverse the assertion that the claim of a second heating with an open ended temperature range is NEW MATTER. Applicants incorporate by reference the arguments advanced on pages 10-12 of the *Response* filed November 19, 1999. Although there are advantages when the reducing step is performed at a temperature lower than 750°C, Applicants believe that the claimed invention is not limited to the this feature. For example, the reducing step is practicable when the second heating is performed at a higher temperature than the described temperature in the specification, e.g. 750°C. If a common material such as quartz is provided as the substrate in the present invention, the reducing step can be performed at a temperature higher than 750°C and advantages of the present invention will not be lost. Accordingly, reconsideration is respectfully requested.

The *Office Action* rejects claims 24-63 under 35 U.S.C. §103(a) as being unpatentable over ***Ohtani et al.*** (U.S. Patent No. 5,543,352) in view of ***Zhang et al.*** (U.S. Patent No. 5,529,937)or visa versa, optionally in view of ***Liu et al. '826*** and ***Zhang et al. '291***. Applicants would like to direct the Examiner's attention to the *Verified English Translation* of Japanese Patent Application No. 6-

225851 filed on June 21, 1999, which established foreign priority for the subject application. Accordingly, the subject application has an effective filing date of August 26, 1994, which predates the filing date of the ***Ohtani et al.*** (November 16, 1994 filing date) patent. In view of the arguments solicited in response to the 35 U.S.C. §112, first paragraph rejection, Applicants submit that no new matter has been added. Consequently, ***Ohtani et al.*** is inapplicable as prior art against the subject application. Withdrawal of the respective prior art rejections based upon ***Ohtani et al.*** is earnestly solicited.

The *Office Action* rejects claims 50-51 and 53-55 under 35 U.S.C. §103(a) as being unpatentable over ***Mitanaga et al.*** (U.S. Patent No. 5,808,321). Applicants respectfully traverse this rejection in view of the remarks advanced hereinbelow.

The claimed invention is directed to a method of fabricating a semiconductor device comprising steps of first heating a amorphous semiconductor film to crystallize the film, reducing defects in the crystallized semiconductor film by second heating the crystallized semiconductor film at a temperature not lower than 450°C after a irradiating step, and then patterning the semiconductor film so as to form a plurality of semiconductor islands.

As the Examiner well knows, three criteria must be met to establish a *prima facie* case of obviousness. *M.P.E.P.* §2143. First, there must be some teaching, suggestion, or motivation to combine or modify the teachings of the prior art to produce the claimed invention, found either in the references themselves or in the knowledge generally available to a skilled artisan. *In re Fine*, 837 F.2d 1071, 5 USPQ.2d 1596 (Fed. Cir. 1988). Second, there must be a reasonable expectation of success. *In re Rhinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976). Third, the prior art must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

Applicants respectfully contend that the *Office Action* has failed to set forth a *prima facie* case of obviousness and that the claimed invention is patentably distinct over the prior art. For instance, while ***Mitanaga*** appears to disclose a second heating step, this second heating step is performed in the step of forming a gate insulating film and <u>after</u> the step of patterning the crystalline silicon film. On the other hand, in the claimed invention, the second heating is performed <u>before</u> a patterning step as set forth in amended claim 50 (and based upon the embodiments 4, 5, and 6). Accordingly, since the proposed ***Mitanaga*** modification fails to expressly teach or implicitly suggest each and every feature of the claimed invention, Applicants respectfully request that the §103

rejection of the pending claims be reconsidered and withdrawn in view thereof.

For at least the reasons expressed hereinabove, Applicants respectfully submit that the pending claims are in condition for allowance, and thus, reconsideration is respectfully requested. Should the Examiner believe any further communications is desirable in order to place the application in even better condition for allowance, he/she is encouraged to contact Applicant's undersigned representative at the telephone number listed below.

Respectfully submitted,

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MARKED-UP COPY OF AMENDED CLAIMS.

24. (Amended) A method of fabricating a semiconductor device comprising steps of:

forming an amorphous semiconductor film over a substrate having an insulating surface;

adding a solution including a catalyst material in contact with said amorphous semiconductor film, said catalyst material being capable of promoting crystallization of said amorphous semiconductor film;

first heating said amorphous semiconductor film to crystallize said amorphous semiconductor film;

irradiating said crystallized semiconductor film with a light to promote further crystallization of said crystallized semiconductor film after said first heating step; and

reducing defects in said crystallized semiconductor film by second heating said crystallized semiconductor film at a temperature not lower than 450°C after said irradiating step[; and then

annealing said crystallized semiconductor film in an atmosphere comprising hydrogen for hydrogenation after said second heating].

32. (Amended) A method of fabricating a semiconductor device comprising steps of:

forming an amorphous semiconductor film over a substrate having an insulating surface;

selectively adding a solution including a catalyst material in contact with a first portion of said amorphous semiconductor film while said solution is not added to a second portion of said amorphous semiconductor film, said catalyst material being capable of promoting crystallization of said amorphous semiconductor film;

first heating said amorphous semiconductor film [so] to crystallize said amorphous semiconductor film so that crystal growth proceeds from said first portion to said second portion in a lateral direction with respect to said insulating surface;

irradiating said crystallized semiconductor film with a light to promote further crystallization of said crystallized semiconductor film after said first heating step; and

reducing defects in said crystallized semiconductor film by second heating said crystallized semiconductor film at a temperature not lower than 450°C after said irradiating step[; and then

annealing said crystallized semiconductor film in an atmosphere comprising hydrogen for hydrogenation after said second heating].

38. (Amended) A method according to claim 32 wherein said [first portion of said crystallized semiconductor film contains said catalyst material at a first concentration of 1 x 10^{16} to 1 x 10^{19} atoms-cm^{-3} while said second portion of said crystallized semiconductor film contains said catalyst material at a second concentration lower than said first concentration] irradiating step is performed in a nitrogen atmosphere.

41. (Amended) A method of fabricating a thin film transistor comprising steps of:

forming an amorphous semiconductor film over a substrate having an insulating surface;

selectively adding a solution including a catalyst material in contact with a first portion of said amorphous semiconductor film while said solution is not added to a second portion of said amorphous semiconductor film, said catalyst material being capable of crystallization of said amorphous semiconductor film;

first heating said amorphous semiconductor film to crystallize said amorphous semiconductor film so that crystal growth proceeds from said first portion to said second portion in a lateral direction with respect to said insulating surface;

irradiating said crystallized semiconductor film with a light to promote further crystallization of said crystallized semiconductor film after said first heating step;

reducing defects in said crystallized semiconductor film by second heating said crystallized semiconductor film at a temperature not lower than 450°C after said irradiating step; and

forming a channel forming region in said semiconductor film using said second portion of the crystallized semiconductor film[; and then

annealing said crystallized semiconductor film in an atmosphere comprising hydrogen for hydrogenation after said second heating].

47. (Amended) A method according to claim 41 wherein said [first portion of said crystallized semiconductor film contains said catalyst material at a first concentration of 1 x 10^{16} to 1 x 10^{19} atoms-cm^{-3} while said second portion of said crystallized semiconductor film contains said catalyst material at a second concentration lower than said first concentration] irradiating step is performed in a nitrogen atmosphere.

50. (Amended) A method of fabricating a semiconductor device comprising steps of:

forming an amorphous semiconductor film over a substrate having an insulating surface;

introducing a catalyst material in contact with said amorphous semiconductor film, said catalyst material being capable of crystallization of said amorphous semiconductor film;

first heating said amorphous semiconductor film to crystallize said amorphous semiconductor film;

irradiating said crystallized semiconductor film with a light to promote further crystallization of said crystallized semiconductor film after said first heating step; and

reducing defects in said crystallized semiconductor film by second heating said crystallized semiconductor film at a temperature not lower than 450°C after said irradiating step; and then

[annealing said crystallized semiconductor film in an atmosphere comprising hydrogen for hydrogenation after said second heating] patterning said semiconductor film so as to form a plurality of semiconductor islands.

56. (Amended) A method of manufacturing a semiconductor device comprising:

forming a semiconductor film comprising amorphous silicon over a substrate having an insulating surface;

crystallizing said semiconductor film by first heating using a catalyst material;

irradiating the crystallized semiconductor film with a pulsed excimer laser light to increase crystallinity of the semiconductor film after said first heating wherein one portion of said semiconductor film is irradiated with a plurality of shots of said pulsed excimer laser light,

reducing defects of the crystallized semiconductor film by second heating at a temperature not lower than 450°C after the irradiation of said laser light.

59. (Amended) A method according to claim 24 wherein said temperature of said second heating is [performed at a temperature] lower than a strain point of said substrate.

60. (Amended) A method according to claim 32 wherein said temperature of said second heating is [performed at a temperature] lower than a strain point of said substrate.

61. (Amended) A method according to claim 41 wherein said temperature of said second heating is [performed at a temperature] lower than a strain point of said substrate.

62. (Amended) A method according to claim 50 wherein said temperature of said second heating is [performed at a temperature] lower than a strain point of said substrate.

63. (Amended) A method according to claim 56 wherein said temperature of said second heating is [performed at a temperature] lower than a strain point of said substrate.

MARKED-UP COPY OF SPECIFICATION CHANGES:

Page 33, second full paragraph:

Thereafter, the substrate is subjected to annealing by laser light irradiation. Although a KrF excimer laser (wavelength: 248 nm; pulse width: 20 nsec) is used in this embodiment, other lasers may also be used. As for the laser light irradiation conditions, the energy density is 200 to 400 mJ/cm^2 , for instance, 250 mJ/ cm^2, and 2 to 10 shots, for instance, 2 shots, are applied per one location. The annealing effect may be enhanced by heating the substrate to 200 to 450°C during the irradiation [(Fig. 6(C))] <u>(Fig. 5(C))</u>.

Page 41, third full paragraph:

Then, the crystalline silicon film 903 is patterned to form an active layer of the TFT. After a 1,000 Å thick silicon oxide film to become a gate insulating film <u>904</u> is formed by plasma CVD, a 5,000 Å thick film mainly made of aluminum is formed and then patterned into a gate electrode 905. A 2,000 Å thick oxide layer 906 is formed around the gate electrode 905 by performing anodic oxidation in an electrolyte with the gate electrode 905 used as the anode.